 **Indian Institute of Technology Patna**

**Dept. of Electrical Engineering**

IIT Patna Campus, Bihta – 801103

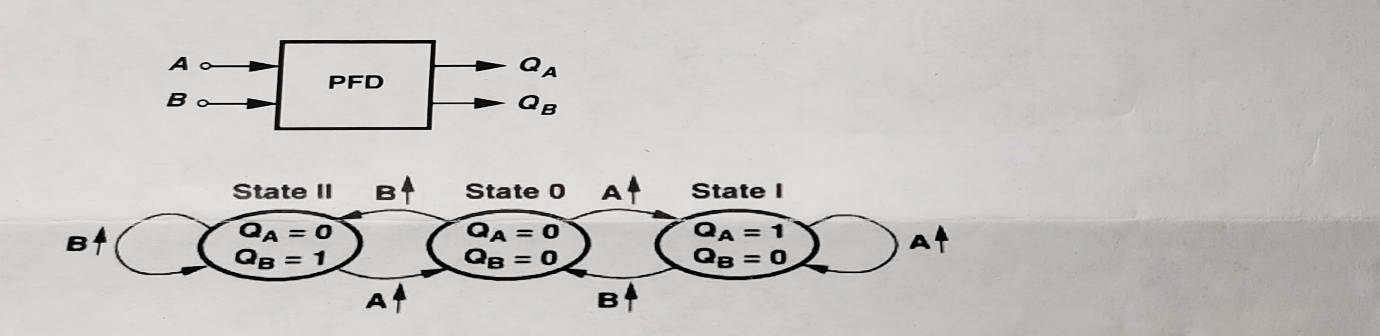
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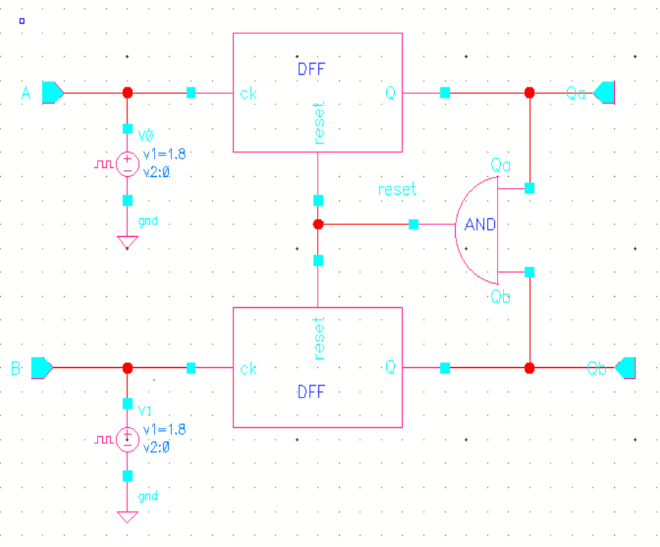
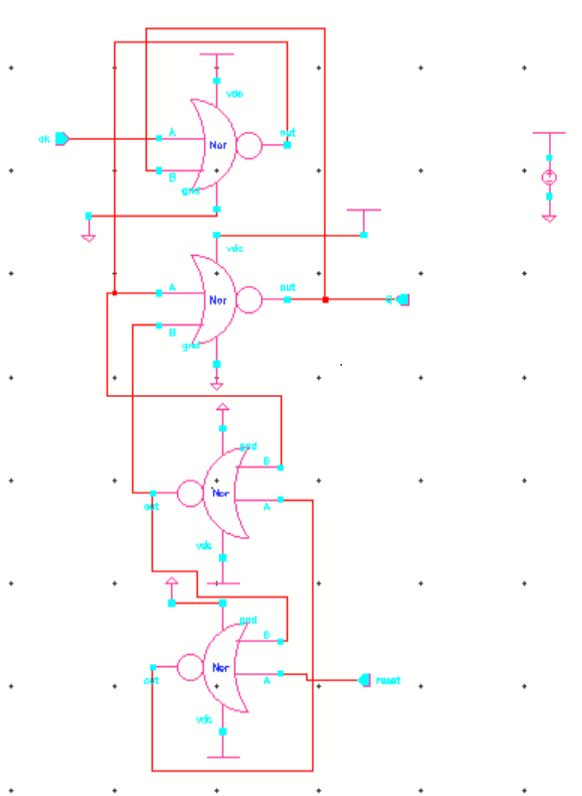
**Project** – Classical PLL

**Theory :** A **Phase Frequency Detector (PFD)** is an essential component of a Phase-Locked Loop (PLL) that compares the phase and frequency of two input signals: a reference signal and a feedback signal from the voltage-controlled oscillator (VCO). It generates two output signals, UP and DOWN, which indicate whether the feedback signal is lagging or leading the reference signal in phase or frequency. These outputs are used to control the charge pump, which adjusts the VCO to align the feedback signal with the reference signal. The PFD operates linearly, enabling precise detection of phase and frequency differences, and it eliminates dead zones, ensuring efficient locking and stability in PLL systems commonly used in communication, clock generation, and frequency synthesis applications.

**Circuit Diagram :**

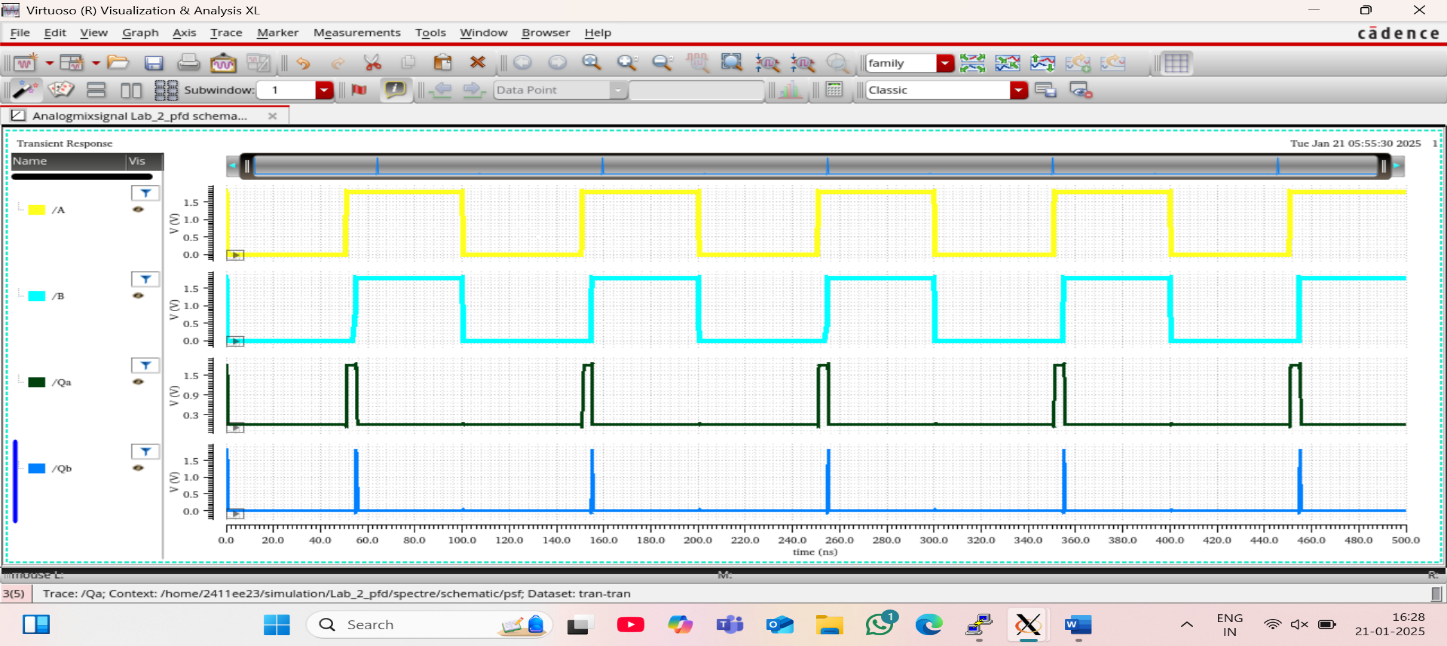


**Fig.1 Block and State Diagrams of a PFD**

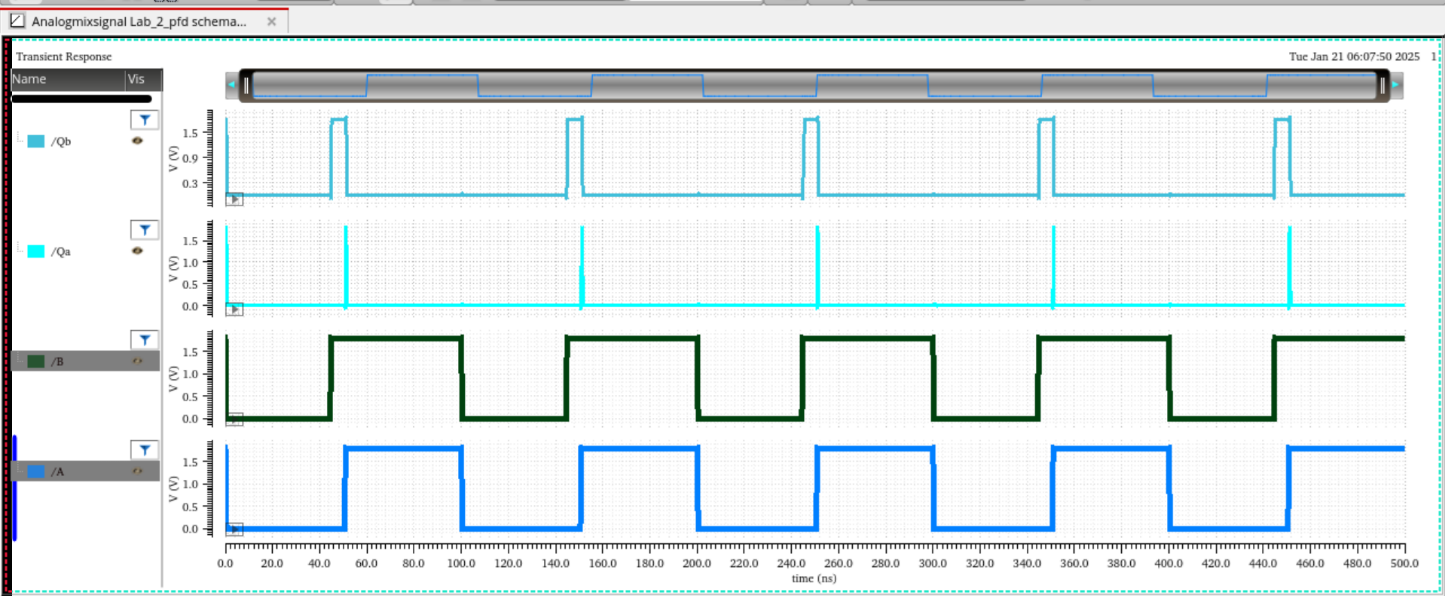
 

**Fig.2 PFD using DFF on cadence Fig.3 A resettable D-FF**

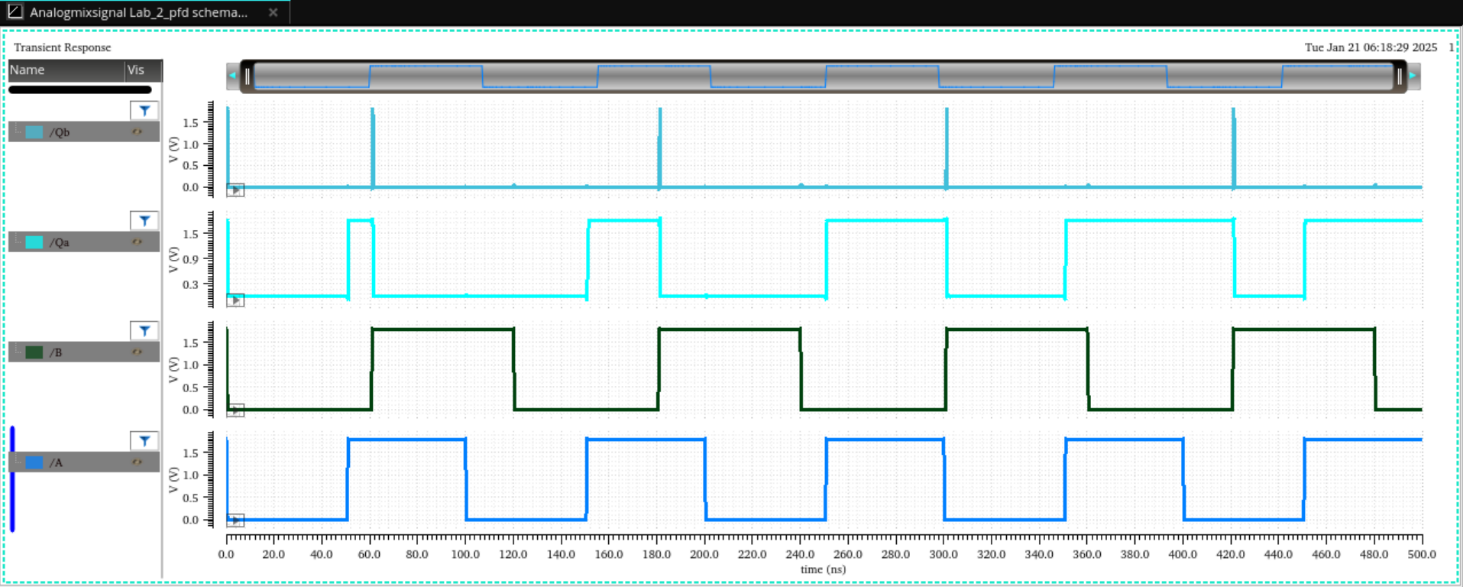
**Result :**

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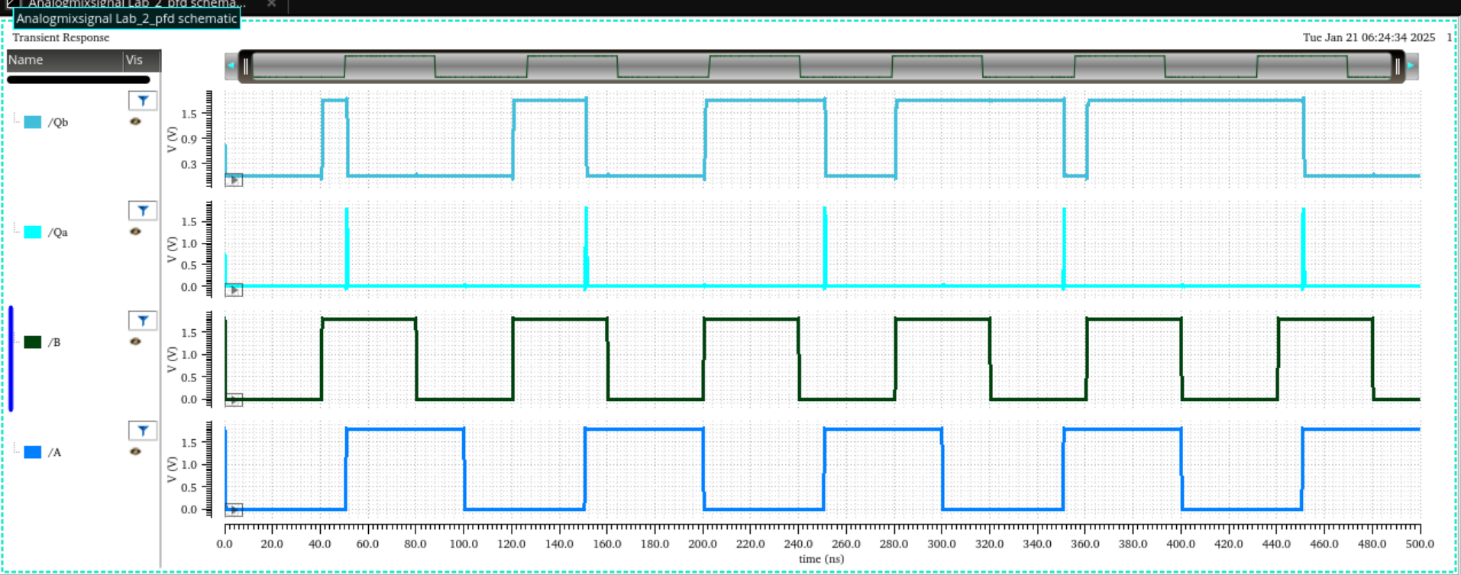
**Fig 1:** Frequencies are equal but A leading B.



**Fig 2:** Frequencies are equal but A lagging B.

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**Fig 3:** Frequency of A > Frequency of B

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**Fig 4:** Frequency of A < Frequency of B